Implementation of Output Capacitorless LDO Regulator Based on Flipped Voltage Follower for Low Power Applications

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***Abstract*—This paper proposes a based flipped voltage follower Output Capacitorless Low-Dropout (OCL-LDO) regulator with voltage spike detection circuit for low power applications. The OCL-LDO regulator introducing a capacitive coupling circuit at the output of the LDO for output voltage spike detection. The detection circuit uses the transient voltage at the output of the LDO to instantaneously increase the charge and discharge current of the improved Flipped Voltage Follower (FVF). The power transistor gate switching rate can be improved to increase the transient response of the LDO. This based flipped voltage follower OCL-LDO regulator with voltage spike detection circuit is designed using TSMC 0.35μm 2P4M CMOS process technology. According to the simulation and measured results, the circuit with chip area is 1.35×1.35mm^2, total chip power dissipation about 0.92mW. Under heavy load condition this chip line regulation is 58mV/V and load regulation is 0.38mV/mA. The chip input supply voltage can operate from 1.6V to 3.3V, the load current from 5mA to 100mA and the output voltage can be stabilized at 1.0V.**

***Index Terms*—Output Capacitorless Low-Dropout (OCL-LDO) regulator, Flipped Voltage Follower (FVF), load regulation, line regulation, Power Supply Rejection Ratio (PSRR)**

I. Introduction

At present, the functions of portable electronic products are updated, and the application is diversified and can be used for a long time toward low power and small area. Therefore, a high-efficiency power management module and a mixed signal circuit are required to be integrated on the same system chip (SOC) to achieve a variety of low power applications. A low-dropout voltage (LDO) regulator, with low noise, small size, and improved performance, is the mainstream of low-power regulation and intelligent power management regulator circuits [1]. Traditional LDO linear regulators require an output filter capacitor of a few microfarads to a dozen microfarad grades as frequency compensation, thus accounting for PCB area and cost. Among all on-chip LDO regulator, the Flipped Voltage Follower (FVF) based LDO regulators are more attractive in terms of simplicity, fast transient responses and low-voltage power consumption [2]. Transient response is a critical dynamic specification in LDO regulator design. Both the amplitude of the voltage spike and the recovery time of the regulated output voltage affect its overall accuracy, which indirectly impacts the performance of the circuits supplied by the LDO. In fact, the transient response of a LDO is related to different design parameters such as the closed-loop stability, the loop bandwidth and the slew rate at the gate of the power transistor [3], [4].

This paper proposes an FVF based output capacitorless (OCL-LDO) regulator architecture that utilizes capacitive coupling as an output voltage spike detection circuit without frequency capacitor compensation. It can be applied to System-on-Chip (SOC) low power applications, and the circuit architecture is shown in Fig. 1. The following is an analysis and design of the OCL-LDO core circuit, the voltage spike detection circuit, the bias current generating circuit and the control voltage generator which constitute the OCL-LDO regulator based on flipped voltage follower circuit.

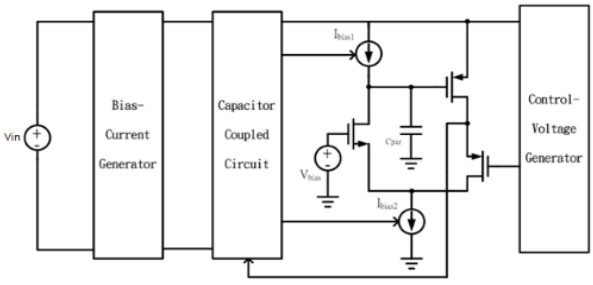

Figure 1. Schematic of FVF based OCL-LDO regulator.

II. Architecture and Circuits Design

The schematic of the proposed OCL-LDO regulator with voltage spike detection circuit for low power applications is shown in Fig. 1. The core circuit of OCL-LDO regulator is basically based on the flipped voltage follower, which is a modified structure of the super source follower as shown in Fig. 2 [5]. V_{IN} is the unregulated input supply voltage of the LDO. M_P is the power transistor, while M_{C1} and M_{C2} form a folded error amplifier in the common-gate configuration. The basic principle of the small-signal negative feedback regulation

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as follow: When power MOS M_P (basic LDO) output current I_O suddenly increases, due to the large C_{par} value (power MOS M_P gate terminal parasitic capacitances), the LDO cannot immediately change the voltage V_{SG} of M_P to supply current, so this situation leads to a decrease in LDO output voltage V_O. The source of the power MOS M_{C1} detects the drop of the LDO output voltage V_O, and generates a falling error voltage at the gate of the power MOS M_P to increase the current from the input power source V_{IN} to the load, so that V_O rises to the basic principle of voltage regulation. Similarly, when I_O suddenly decreases, the LDO cannot immediately reduce the voltage V_{SG} of M_P and raises V_O. Due to the performance of the negative feedback common-gate amplifier, the rising error voltage is generated at the gate of the power MOS M_P to reduce the current from the input power source V_{IN} to the load, so that V_O is lowered to achieve the closed-loop regulated LDO output. As a result, the transconductances of M_{C1} and M_{C2} should be large in order to improve the small-signal response.

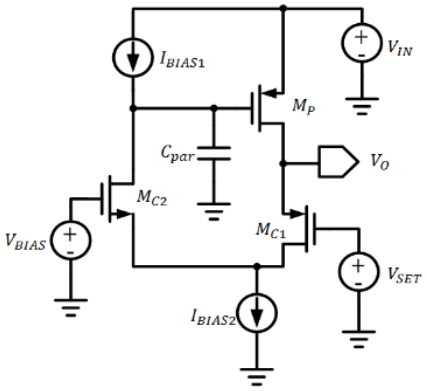


Figure 2. OCL-LDO core circuit.

The OCL-LDO undergoes large-signal response when there is rapid and large change of output load current I_O. When I_O rapidly increases, the LDO cannot change V_{SG} of M_P instantaneously to provide current due to the large C_{par}, and this situation causes to drop V_O. The drop of V_O reduces V_{SG} of M_{C1}, and it causes M_{C1} to cut-off momentarily. Thus, $I_{BIAS2} - I_{BIAS1}$ is the discharging current of C_{par}. The gate of the power PMOS M_P drops rapidly to instantaneously increase the current from the input power source V_{IN} to the load, so that the fast V_O rises to achive the basic principle of voltage regulation. Conversely, when I_O suddenly decreases a lot, the LDO cannot immediately reduce the V_{SG} of M_P and raises V_O. The sudden increase in V_O causes the source voltage of M_{C1} to increase. Due to the performance of the common-gate amplifier, the drain of M_{C1} and the gate voltage of M_{C2} increase almost suddenly. This causes M_{C2} to be cut-off immediately. Therefore, the charging current of C_{par} is I_{BIAS1}. The gate of the power PMOS M_P rises rapidly to instantaneously reduce the current from the input power source V_{IN} to the load, so that the fast V_O drops to achives the voltage regulation performance.

The following is the analysis and design of the output voltage spike detection circuit, the bias current generating circuit and the control voltage generator circuit which constitute the OCL-LDO regulator based on flipped voltage follower circuit.

A. *Output Voltage Spike Detection Circuit*

From the above analysis, both I_{BIAS1} and I_{BIAS2} determine slew rate of the closed loop of the OCL-LDO. Higher bias current does enhance the transient response of the LDO, but this approach consumes unnecessary power dissipation. The OCL-LDO introducing a capacitive coupling circuit at the output of the LDO for output voltage spike detection. The detection circuit makes use of the rapid transient voltage at the LDO output to increase the bias current momentarily. Their circuit implementations are shown in Fig. 3. The MOS transistors M_{UP1}, M_{UP2} and M_{UP3} provide I_{BIAS1} to the OCL-LDO shown in Fig. 1, while the MOS transistor $M_{DN1} \sim M_{DN3}$ give I_{BIAS2}. The coupling capacitors, C_{UP} and C_{DN}, as well as two resistors, R_{UP} and R_{DN}, are to form the proposed output voltage spike detection circuit of the OCL-LDO regulator. One of the two terminals of both C_{UP} and C_{DN} are connected to V_O in order to achieve direct detection of the voltage spikes created at the transient instant.

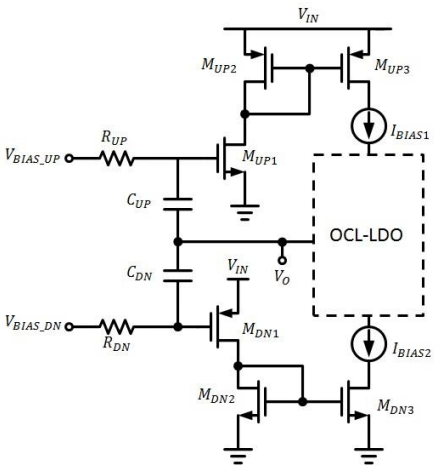


Figure 3. High-pass RC voltage spike detection circuit.

B. *Bias Current Generator Circuit*

The bias current generator designed in this paper is shown in Fig. 4, and it provides the two working bias voltages $V_{BIAS,UP}$ and $V_{BIAS,DN}$ for the voltage spike detection circuit. To make the bias current generator independent of the supply voltage, the regulated output voltage of the

OCL-LDO is used for the bias-current generation. The bias current is given by, $I_{BIAS}=(V_o-V_{GS,B})/R_B$.

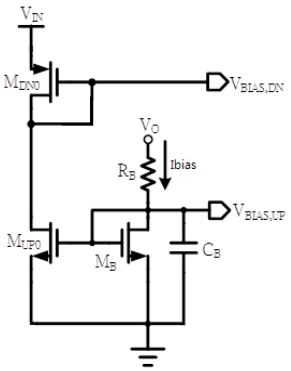


Figure 4. Bias current generator circuit.

A decoupling capacitor (C_B) is used to stabilize I_{BIAS}. In this paper, the transient response of the OCL-LDO core circuit needs to increase the slew rate of the closed loop of LDO. The charging and discharging currents, I_{BIAS1} and I_{BIAS2}, are also determined by the bias current generating circuit. At the same time, once the current I_{BIAS} is determined, the bias voltage $V_{BIAS,UP}=V_{GS,B}$ and $V_{BIAS,DN}=V_{IN}-V_{SG,DN0}$ of the voltage spike detection circuit can also be determined.

C. Control Voltage Generator Circuit

The control voltage V_{SET} of the core circuit of the OCL-LDO is generated by the control voltage generator of Fig. 5. The control voltage generator is essentially an amplifier with negative feedback [5], [6]. The reference voltage V_{REF} of this error amplifier is typically provided by a bandgap reference voltage circuit (BGR) with independent temperature and supply voltage. Because the source voltage $V_{S,C1}$ of M_{C1} of the OCL-LDO core circuit in Fig. 2 is connected to the output of the LDO, making $V_O=V_{SET}+V_{SG,C1}$.

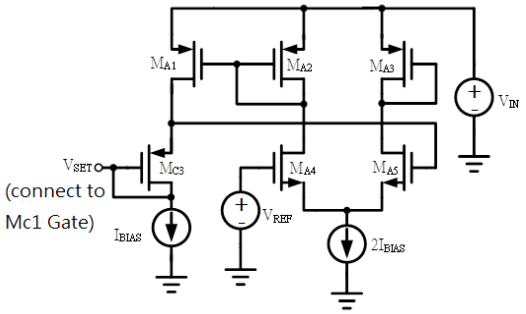


Figure 5. Control voltage generator circuit.

The two input terminals of the differential input pair (M_{A4}, M_{A5}) of the control voltage generator are respectively connected to the reference voltage V_{REF} and the source voltage $V_{S,C3}$ of M_{C3}, so $V_{SET}=V_{REF}-V_{SG,C3}$. Therefore, if the aspect ratio sizes of the two MOS transistors M_{C1} and M_{C3} are the same, and the bias currents of the two MOS transistors M_{C1} and M_{C3} are the same, the bias current is designed as I_{BIAS} in this paper, so $V_{S,C1}=V_{SG,3}$, the output voltage of the OCL-LDO core circuit is $V_O=V_{REF}$.

After summarizing the analysis and design of all component circuits, the physical detail circuit and the layout micrograph of the proposed OCL-LDO regulator with voltage spike detection circuit for low power applications are shown in Fig. 6 and Fig. 7, respectively.

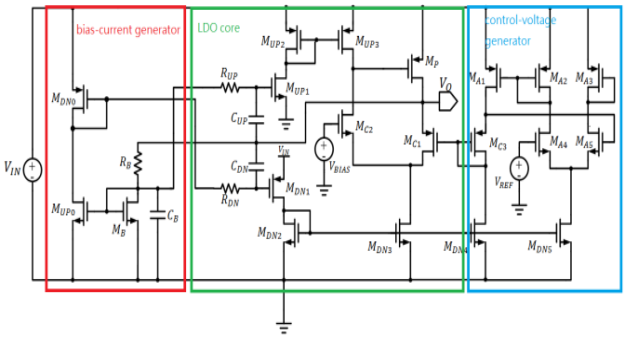


Figure 6. Proposed OCL-LDO regulator based on FVF circuit.

And the chip size is about $1.35\times1.35mm^2$, total chip power dissipation about $0.922mW$ [7].

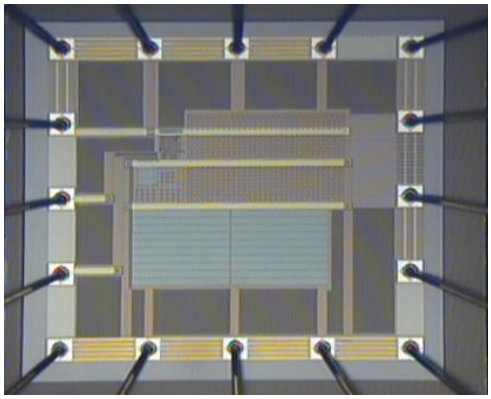


Figure 7. Micrograph of the OCL-LDO circuit.

III. Simulation and Measured Results

By using TSMC 0.35μm CMOS 2P4M process to simulate the designed OCL-LDO regulator with voltage spike detection circuit for low power applications, the results of the post-simulation under five different corners are shown below.

Fig. 8 shows the output voltage waveforms of the OCL-LDO regulator operate at full load condition $I_{Load}=100mA$, the input supply voltage of the OCL-LDO regulator circuit gradually increases from $0V$ to $3.3V$. The simulated result shows the output voltage of the OCL-LDO regulator can stable at $1.0V$ steadily under five different corners with the range of input supply voltage from $1.6V$ to $3.3V$ (The error is about 5%).

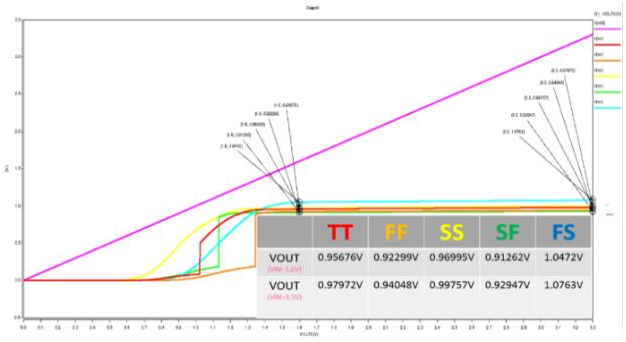
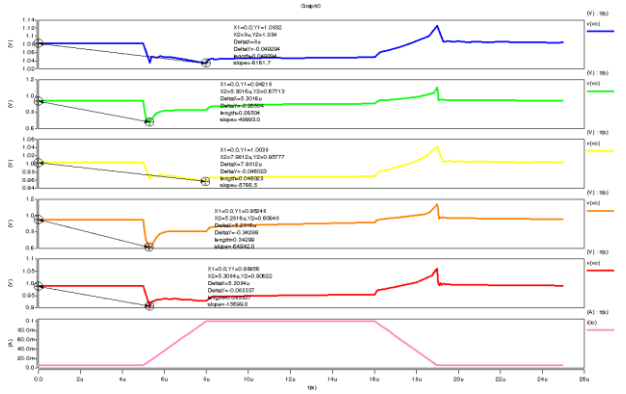
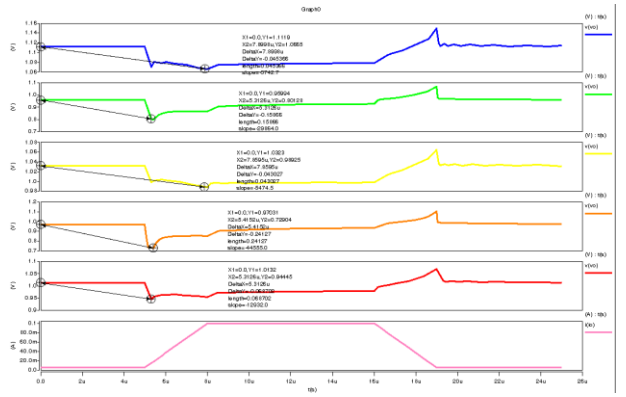


Figure 8. Input supply voltage range of OCL-LDO circuit.

Fig. 9(a) and (b) show the load regulation of the OCL-LDO regulator circuit is about $0.95mV/mA$ ($V_{in}=1.6V$) and $0.87mV/mA$ ($V_{in}=3.3V$), under the input voltage is fixed at $1.6V$ and $3.3V$ respectively, and which load current instantaneous variation from $50mA$ to $500mA$. The OCL-LDO regulator output voltage can stable at $1.0V$ steadily, and the steady-state time is $3.85us$ ($V_{in}=1.6V$) and $3.63us$ ($V_{in}=3.3V$), respectively.



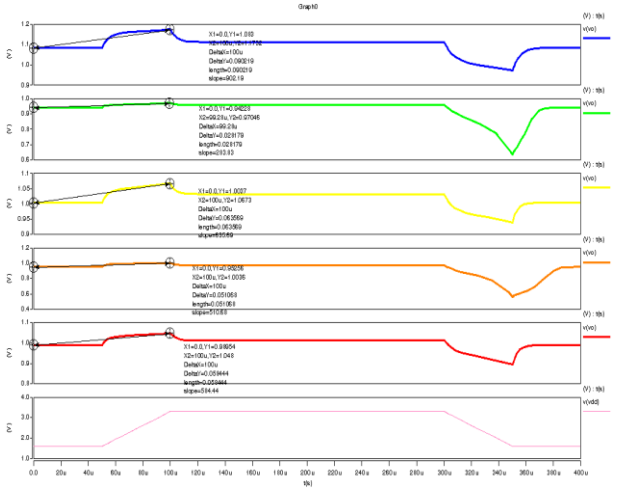
(a) $V_{IN}=1.6V$



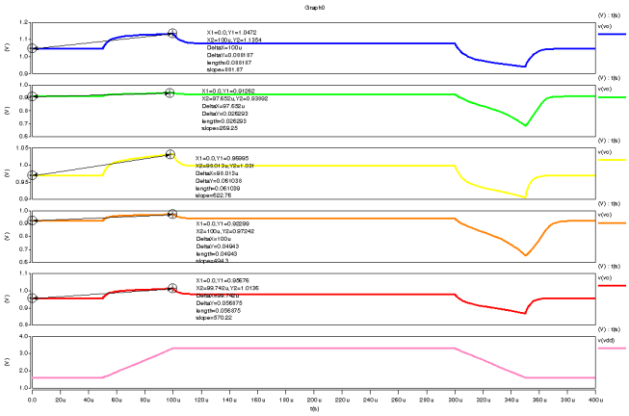
(b) $V_{IN}=3.3V$

Figure 9. Load regulation of circuit [I_{Load} change from $5mA$ to $500mA$ for different input voltage source].

Fig. 10(a) and (b) show the line regulation of the OCL-LDO regulator circuit is about $38.6mV/V$ ($I_{Load}=5mA$) and $32.4mV/V$ ($I_{Load}=100mA$), under the output is connected to light load ($I_{Load}=5mA$) and full load ($I_{Load}=100mA$) condition respectively, and which input supply voltage instantaneous variation from $1.6V$ to $3.3V$ at time of $50us$ and variation from $3.3V$ to $1.6V$ at the time of $300us$. The OCL-LDO regulator output voltage can stable at $1.0V$ steadily, and the steady-state time is $64.5us$ and $74.5us$, respectively.



(a) $I_{Load}=5mA$



(b) $I_{Load}=100mA$

Figure 10. Line regulation of circuit [V_{IN} change from $1.6V$ to $3.3V$ for different load current condition].

Fig. 11 gives the post-simulation results of the power supply rejection ratio (PSRR) of the proposed OCL-LDO regulator circuit. And shown in figure, in the DC region, the PSRR is about -50dB. At the frequency 100KHz, the the PSRR is about -20dB.

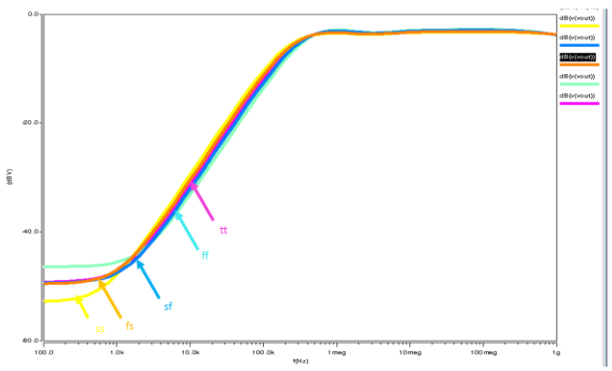


Figure 11. Power supply rejection ratio of OCL-LDO circuit.

The PCB board for chip characteristics measurement is shown in Fig. 12.

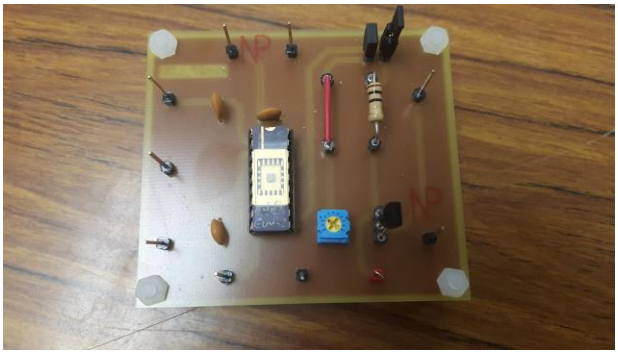
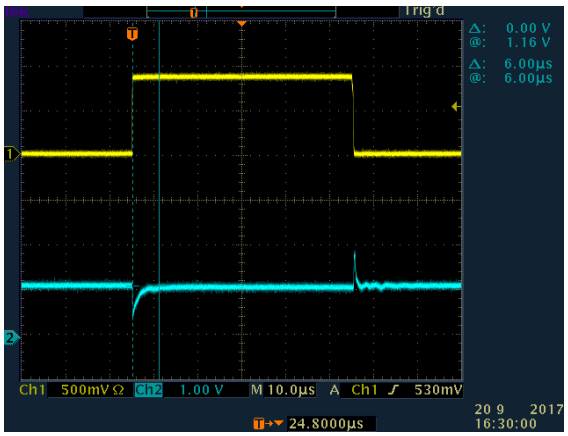
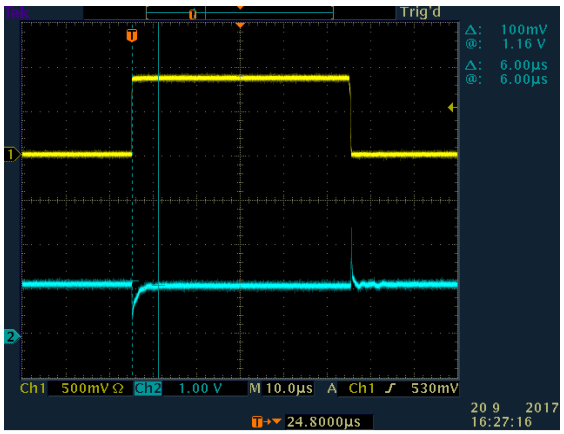


Figure 12. Measurement PCB of chip function test.

Fig. 13 (a) and (b) show the load regulation measured results of the OCL-LDO regulator circuit, where the output voltage can stable at $1.0V$ steadily, and the steady-state time is $6us$. The variation of output voltage of the OCL-LDO regulator is about $60mV$ ($V_{IN}=1.6V$) and $89mV$ ($V_{IN}=3.3V$), respectively.



(a) $V_{IN}=1.6V$

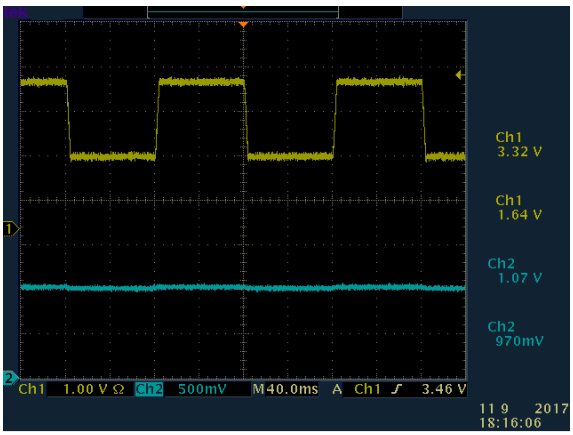


(b) $V_{IN}=3.3V$

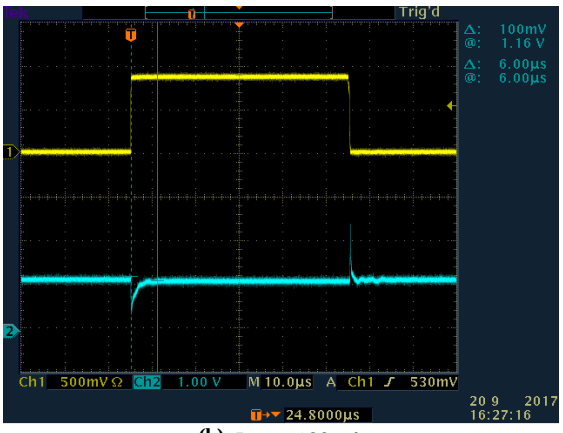
Figure 13. Load regulation measured results of chip [I_{Load} change from $5mA$ to $100mA$].

And the load regulation of the chip is $0.387mV/mA$, when the load current instantaneous variation from $5mA$ to $100mA$. Where shown in Fig. 13, yellow and blue lines represent the measurement data of load current condition (from $5mA$ to $100mA$) and output voltage ($V_O=1.0V$) of the OCL-LDO regulator.

Fig. 14 (a) and (b) show the line regulation measured results of the OCL-LDO regulator circuit, where the variation of output voltage is from $0.97V$ to $1.07V$ ($I_{Load}=5mA$) and from $0.93V$ to $1.03V$ ($I_{Load}=100mA$), respectively. The chip output voltage can stable at $1.0V$ steadily and its line regulation is about $58mV/V$ when the input supply voltage instantaneous variation from $1.6V$ to $3.3V$. Where shown in Fig. 14, yellow and blue lines represent the measurement data of the input supply voltage from $1.6V$ to $3.3V$ and the chip output voltage is ($V_O=1.0V$).



(a) $I_{Load}=5mA$



(b) $I_{Load}=100mA$

Figure 14. Line regulation of measured results of chip [V_{IN} change from $1.6V$ to $3.3V$].

Fig. 15 gives the measured results of the Power Supply Rejection Ratio (PSRR) of the proposed OCL-LDO regulator circuit by the frequency response analyzer (Bode 100 R2). And shown in Fig. 15, red lines represent the measured PSRR of the proposed OCL-LDO regulator circuit. In the DC region, the PSRR is about -50dB. At the frequency 100KHz, the PSRR is about -25dB. Different circuit topologies operating at various frequencies induce significant fluctuations on the power supply. These variations present a critical challenge, especially in low power LDO regulators based on FVF

structures design [8], [9]. In consequence, it is required to optimize the conflict of aims between high PSRR and low power consumption while maintaining high accuracy.

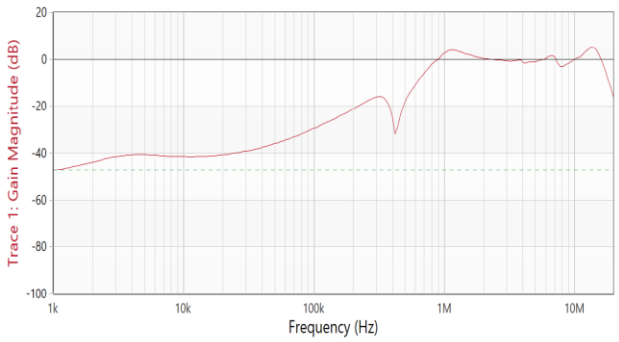


Figure 15. PSRR measured result of chip.

IV. Conclusions

Based on the aforementioned discussions, we can conclude that the implemented OCL-LDO regulator circuit has the chip size is $1.35\times1.35mm^2$ with power dissipation about $0.922mW$. And the simulation and actual measured results of the OCL-LDO regulator circuit are summarized in Table I below. The load regulation and line regulation of the circuit are about $0.38mV/mA$ and $58mV/V$, respectively. The chip input supply voltage can operate from $1.6V$ to $3.3V$, the load current can supply from $5mA$ to $100mA$ and the output voltage can be stabilized at $1.0V$. So, this circuit is suitable for the low power SOC power management module applications. But the PSRR of the proposed OCL-LDO regulator is not sufficient in biomedical or RFID applications for example. Therefore, improve the PSRR of this OCL-LDO at low and high frequency range is future research focus.

TABLE I. Comparison of Expected Specifications, Simulation and Measurement Results

Parameter	Specification	Pre-Simulation	Post-Simulation	Measured Result
Input Voltage Range (V)	1.6~3.3	1.6~3.3	1.6~3.3	1.6-3.3
Output Voltage (V)	1	1.009	0.95676	1.02
Max. Load Current I_{load}(max) (mA)	100	101.34	96	95
Min. Load Current I_{load}(min) (mA)	5	5.11	4.9	4.6
Line Regulation (Io=100mA) (TT)	40 mV/V	45.1 mV/V	29.85 mV/V	58.82 mV/V
Load Regulation (TT)	0.5 mV/mA	1 mV/mA	0.87 mV/mA	0.378 mV/mA

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